Abstracts

Stability and Reliability Investigation on Fully ECL Compatible High Speed GaAs Logic ICs

Y. Hosono, H. Sato, Y. Mima, S. Ichikawa, H. Hirayama, K. Katsukawa, K. Ueda, K. Uetake, T. Noguchi and H. Kohzu. "Stability and Reliability Investigation on Fully ECL Compatible High Speed GaAs Logic ICs." 1987 Microwave and Millimeter-Wave Monolithic Circuits Symposium Digest 87.1 (1987 [MCS]): 49-52.

The electrical characteristics stability and reliability were investigated on newly developed high speed GaAs logic ICS. A resistor-loaded source-coupled FET logic (SCFL) was employed as a basic circuit architecture. The selectively epitaxial grown n/sup +/ - GaAs layers were aclopted for the contact regions of the WSi self-aligned gate FET. Maximum operating data rate of more than 2.6 Gb/s was achieved in these devices, guaranteeing sufficient supply voltage and phase margin. No failure has been observed in DC bias test for 3,000 hours and in RF operational test at 2 Gb/s for 7,000 hours.

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